

**Digital Logic Lab Assignment # 17**

1. **To verify the operation of:**

* **4-bit Shift Register**
* **Types of Registers**

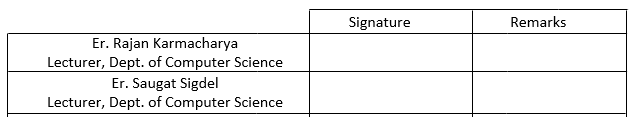
**Submitted By**

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Year I / SEM I

017BSCIT014

**Submitted To**



**OBJECTIVE 1.1**

**To verify the operation of a 4-bit Shift Register**

**THEORY:**

Register is a group of storage cells suitable for holding binary operation. A group of Flip Flops (FF) constitutes a register since each FF is a binary cell capable of storing 1 bit of information. An n bit register has a group of n FFs and is capable of storing any binary information containing n bits. A register may also have combinational gates to perform certain data processing task.

**Shift Register:**

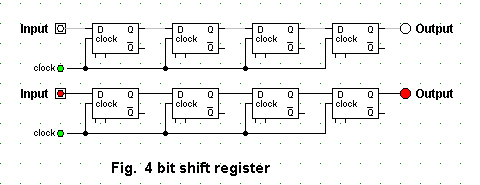
A register capable of shifting its binary information either to the right or the left is Shift Register. The logical configuration of a shift register consists of a chain of FFs connected in cascade with the output of one of FF connected to the input of next FF. All FFs receive common clock pulse which causes the shift of bits.

  Each CP shifts the contents of the register one bit position to the right. The serial input determines what goes into the leftmost FF during the shift. The serial output is taken from the output of the rightmost FF prior to the application of a pulse.

**Circuit Diagram:**

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**Observation:**

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**Conclusion:**

Thus, a 4-bit shift register was constructed.

**OBJECTIVE 1.2**

**To Construct a Serial In Serial Out Register**

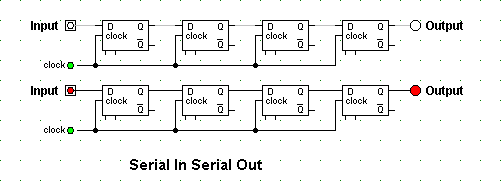
**THEORY:**

It accepts data serially i.e. 1 bit at a time on a single line and produces the stored information on its output in serial form.

**Circuit Diagram:**

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**Observation:**

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**Conclusion:**

Therefore, the serial in serial out register was constructed.

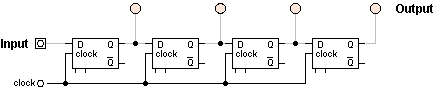
**OBJECTIVE 1.3**

**To Construct a Serial In Parallel Out Register**

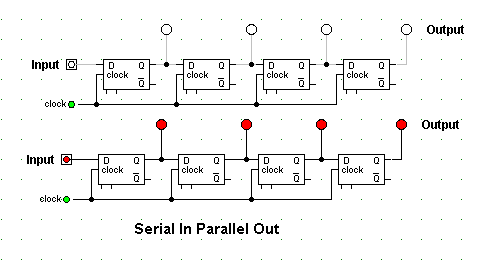
**THEORY:**

Data bits are entered serially into the register with rightmost bit first and all the bits are available simultaneously at the output.

**Circuit Diagram:**

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**Observation:**

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**Conclusion:**

Therefore, the serial in parallel out register was constructed.

**OBJECTIVE 1.4**

**To Construct a Parallel In Serial Out Register**

**THEORY:**

For registers with parallel data inputs, the bits are entered simultaneously into their respective stages on parallel lines.

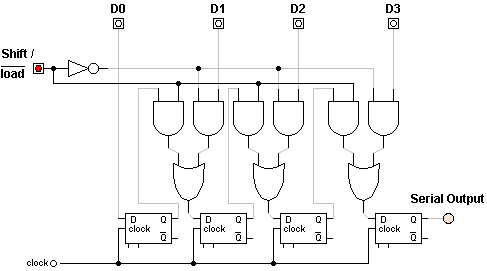
There are 4 data input lines: D0, D1, D2, D3.

Shift/ (Load)’ input

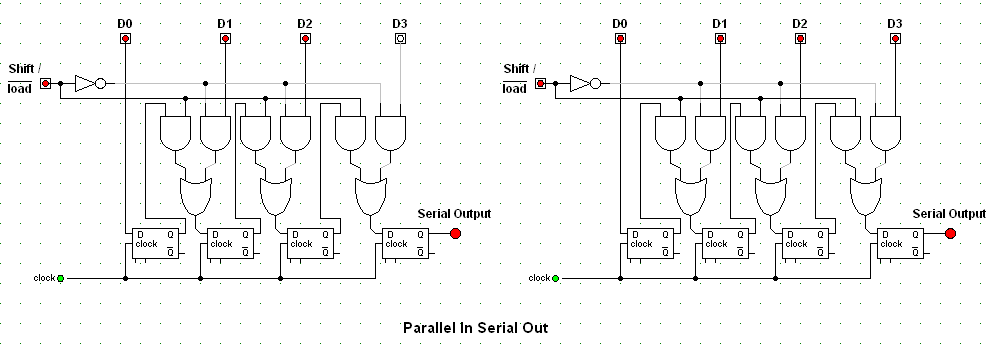
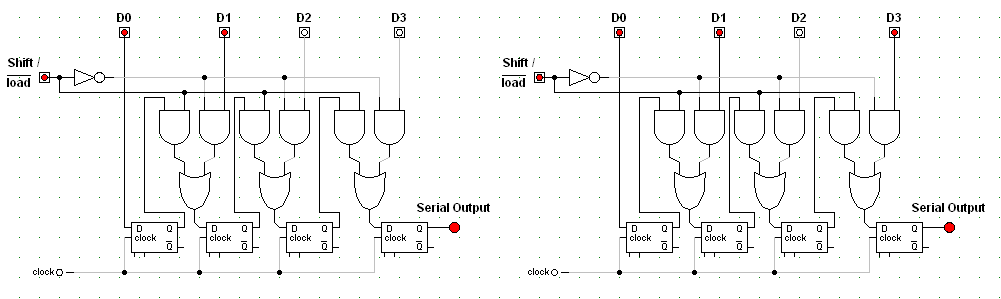
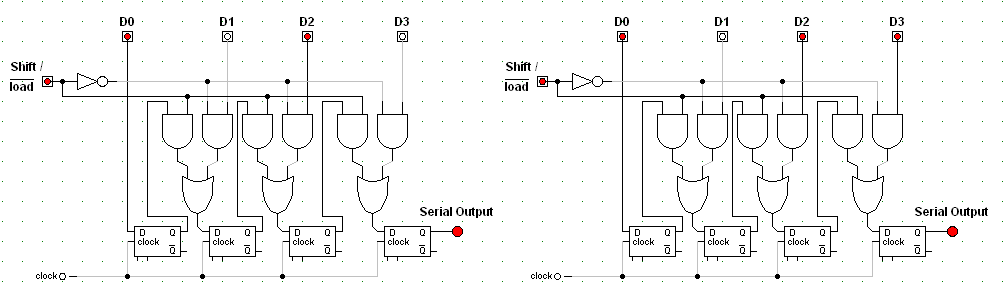
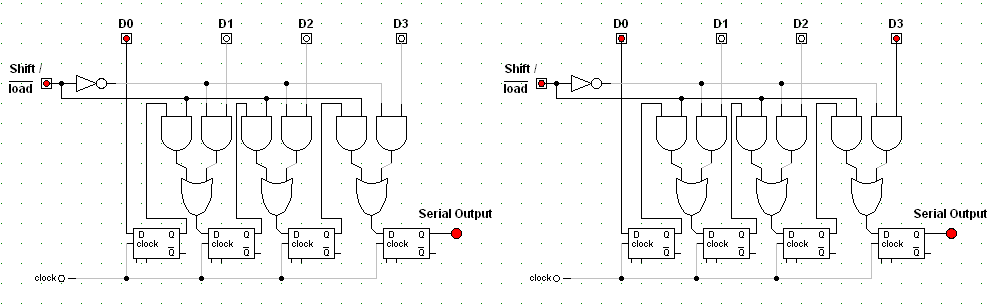
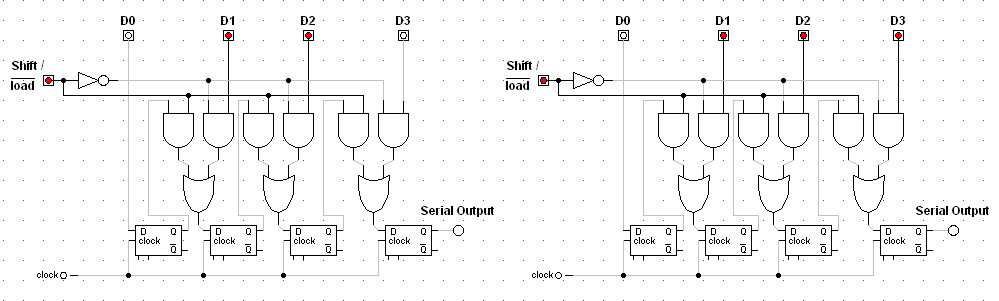
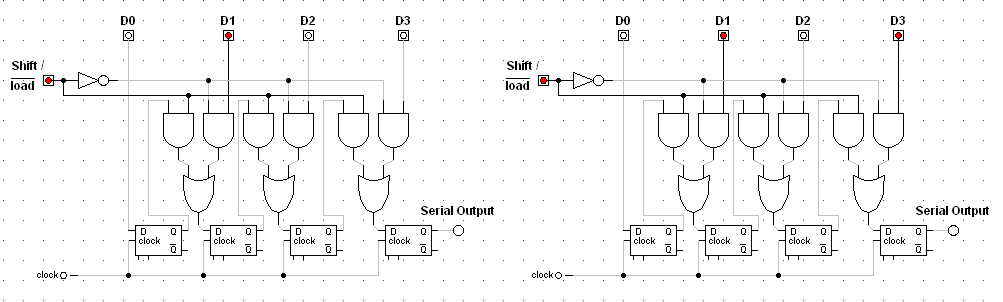
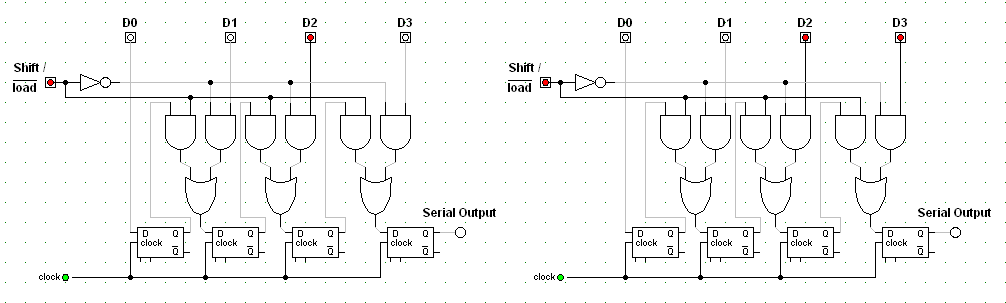
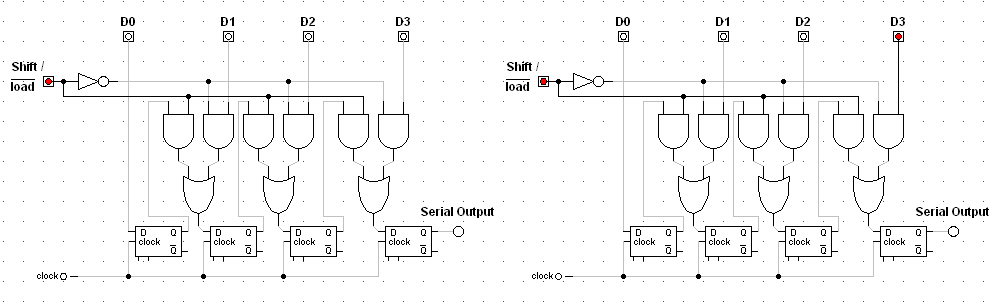
Shift/ (Load)’ = 0: gates 1, 2 and 3 enabled

         Allows data bits to shift right from one stage to next OR gate allows either normal shifting operation or the parallel data entry operation.

**Circuit Diagram:**

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**Observation:**



**Conclusion:**

Therefore, the parallel in serial out register was constructed.

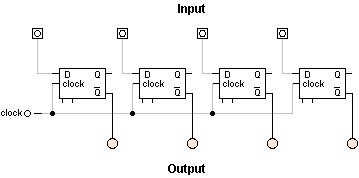
**OBJECTIVE 1.5**

**To Construct a Parallel In Parallel Out Register**

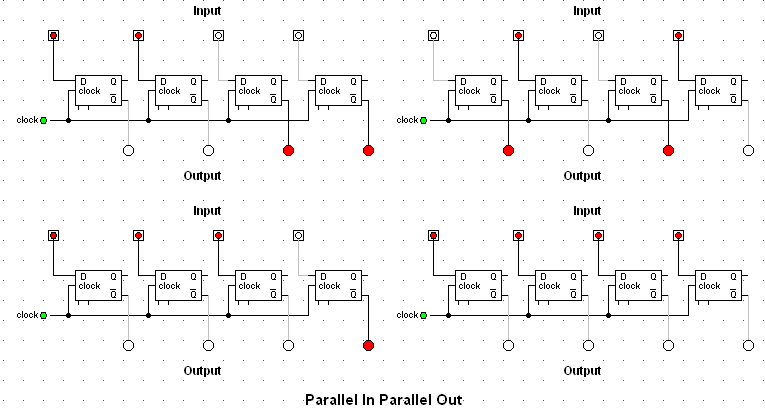
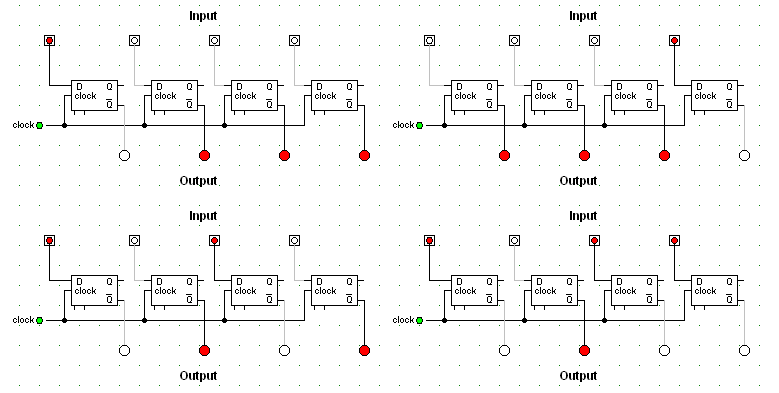
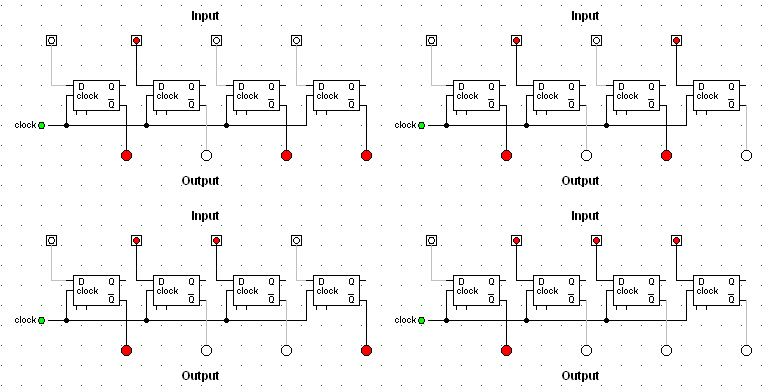
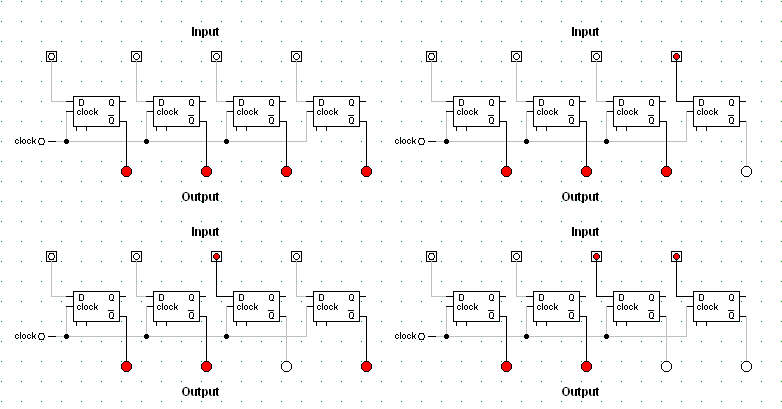
**THEORY:**

Parallel input and output of data

**Circuit Diagram:**

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**Observation:**

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**Conclusion:**

Therefore, the parallel in parallel out register was constructed.